27.4 A CMOS Imager with Column-Level ADC Using Dynamic Column FPN Reduction

M.F. Snoeij, A. Theuwissen, K. Makinwa, J.H. Huijsing

Delft University of Technology, Delft, The Netherlands

A CMOS imager with column-level ADC is presented that uses a dynamic column FPN-reduction technique. It requires 5 extra transistor switches per column and minimal digital overhead at chip level. The technique relaxes the uniformity requirements of column-level ADCs, which can decrease power consumption and chip area. A prototype is realized in a 0.18μm CMOS process. Measurements show that the technique can make a column FPN of ±0.67% nearly invisible to the human eye.

The demand for high-resolution low-cost cameras-on-a-chip has fuelled the development of CMOS imagers with resolutions in the mega-pixel range. The increasing resolution increases the pixel output rate, which makes it difficult to digitize the sensor output using only a single ADC at chip level. Therefore, column-level ADCs are becoming an attractive read-out architecture for high-resolution CMOS imagers. However, if there is a mismatch between the column ADCs, this will lead to column FPN in the image, which may severely degrade the perceived image quality. Column FPN can be observed as vertical stripes in an image that are visible even if the magnitude of the column FPN is much lower than the pixel FPN and/or temporal noise present in an image, such as white noise and photon shot noise. Although it is hard to quantify this perceptual difference between pixel and column FPN, it has been proposed [1] that random column FPN is 5 times more harmful to the perceived image quality than pixel FPN. Therefore, since pixel FPN is typically around 0.5%, a column FPN of about 0.1% or less is necessary to get a sufficiently high perceived image quality.

Previous work [2, 3] has shown that it is possible to realize a column-level ADC with sufficient column-to-column uniformity as to not produce any visible artifacts. However, the demand of less than 0.1% column FPN puts a severe design constraint on the column circuit, which may lead to higher power consumption and larger chip area, as well as a lower yield. The reduction technique proposed in this paper relaxes the column circuit design requirements, thereby potentially reducing power consumption and chip area.

The basic insight behind the proposed reduction technique is that the problem is not the magnitude of column FPN, but its spatial correlation, i.e. every column of the imaging array has a systematic error. This spatial correlation can be removed by putting a switching matrix between the column buses of the pixel array and the rest of the column circuitry, as illustrated in Fig. 27.4.1 [4]. At the beginning of each line time, the state of the switching matrix is changed before the pixel array is read out. As a result of this dynamic column switching (DCS), each column circuit is used to read out not just one, but several columns of the imaging array, thus averaging the non-uniformity of the column circuit over several array columns. Since the switching matrix dynamically changes the relationship between the columns and the column circuits, some extra circuitry is required to perform the inverse operation. This can be easily done on-chip in the digital domain.

In implementing the switching matrix, there is a trade-off between the complexity of the switching matrix versus the reduction of visible column FPN. Simulation results show that when the column FPN is assumed to be random, interchanging 3 adjacent column circuits between 3 column buses is sufficient to render a column FPN of 1% invisible. To achieve this, the switching matrix, as depicted in Fig. 27.4.2, is used. Three transistors are used in each column to connect the column bus to one of the 3 intermediate nodes (n1, n2, n3) that are shared between 3 columns. Two more transistors are used to connect one of the intermediate nodes to the column circuit. As a result, 6 different connections can be made. A digital pseudo-random generator and decoder drives control lines sel1 to sel5, thus changing the state of the switching matrix once every line time. The amount of spatial averaging is further increased by interleaving 2 of the circuits depicted in Fig. 27.4.2, i.e., one circuit is connected to column 1, 3, and 5 while the other one is connected to column 2, 4, and 6.

The switching matrix is implemented in a CMOS imager with a column-level single-slope ADC. A chip micrograph of the 0.18μm CMOS prototype is depicted in Fig. 27.4.7. It has an array of 680×512 pixels; however, in this prototype, only half of the pixel columns are read-out, reducing the effective resolution to 340×512 pixels. For flexibility, the digital hardware that drives the switching matrix and re-orders the digital output is implemented off-chip. The column-level ADC has a single-slope architecture that uses an aggressive low-power comparator design (3.2μW) [5]. For the measurements, an offset-correction step in the column ADC is intentionally omitted, causing high non-uniformities. Figures 27.4.3 and 27.4.4 show raw acquired images with and without DCS. For these images, 20 frames are averaged to reduce temporal noise. The horizontal bands in the image are caused by the fact that different pixel architectures are used in the array, for purposes outside the scope of this paper. Column FPN is clearly visible throughout the picture in Fig. 27.4.3. However, Fig. 27.4.4 shows that dynamic column switching strongly reduces the visibility of column FPN. To quantify the amount of column FPN present, a portion of the image corresponding to a single pixel architecture is measured in uniform light input, as depicted in Figs. 27.4.5a and 27.4.6a. To increase the visibility of the column FPN, the contrast in both images is enhanced 15 times. Using these images, graphs of the averaged column outputs are made (Figs. 27.4.5b and 27.4.6b). The average initial column FPN is ±0.67% (standard deviation); by using the proposed column FPN reduction technique, this is reduced to ±0.41%. The initial peak FPN is 2.7%, and this is reduced to 1.1%.

Acknowledgements:
The authors thank A. Mierop and M. Pertijs for the useful discussions that contributed to this work. The authors also thank Philips Semiconductors for fabrication of the prototype.

References:

[1] D. Sackett, "CMOS Pixel Device Physics," *2005 ISSCC Advanced Circuit Design Forum: Characterization of Solid-State Image Sensors*, Feb., 2005.

[2] T. Sugiki, et al. , "A 60 mW 10b CMOS Image Sensor with Column-to-Column FPN Reduction," *ISSCC Dig. Tech. Papers*, pp. 108-109, Feb., 2000.

[3] K. Findlater, et al., "SXGA Pinned Photodiode CMOS Image Sensor in 0.35μm Technology," *ISSCC Dig. Tech. Papers*, pp. 218-219, Feb., 2003.

[4] T. Anaxagoras, S. Triger, N.M. Allinson, R. Turchetta, "APS Column Fixed Pattern Noise Reduction," *IEEE Workshop on CCDs and Advanced Image Sensors*, pp. 76-79, June, 2005.

[5] M.F. Snoeij, A.J.P. Theuwissen, J.H. Huijsing, "A 1.8V 3.2μW Comparator for Use in a CMOS Imager Column-Level Single-Slope ADC," *IEEE ISCAS*, pp. 6162-6265, May, 2005.

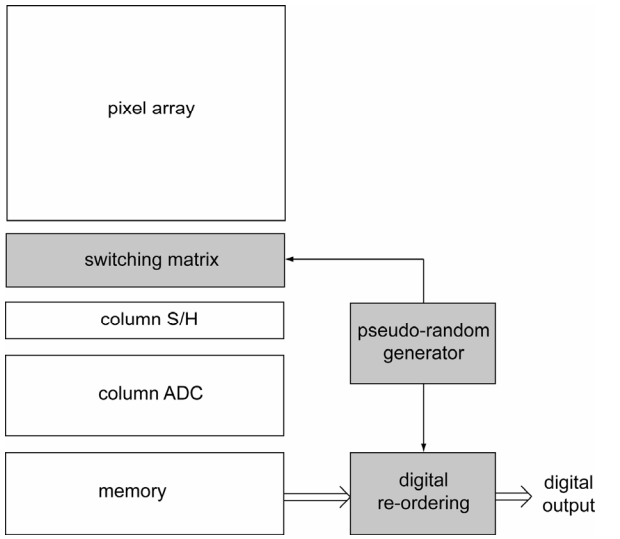

Figure 27.4.1: Block diagram of the sensor (the grey blocks are added to implement DCS).

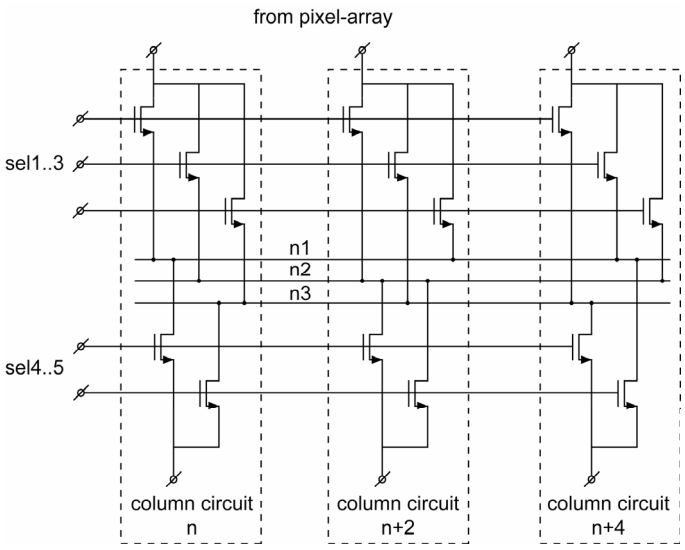

Figure 27.4.2: 3×3 switching matrix element.

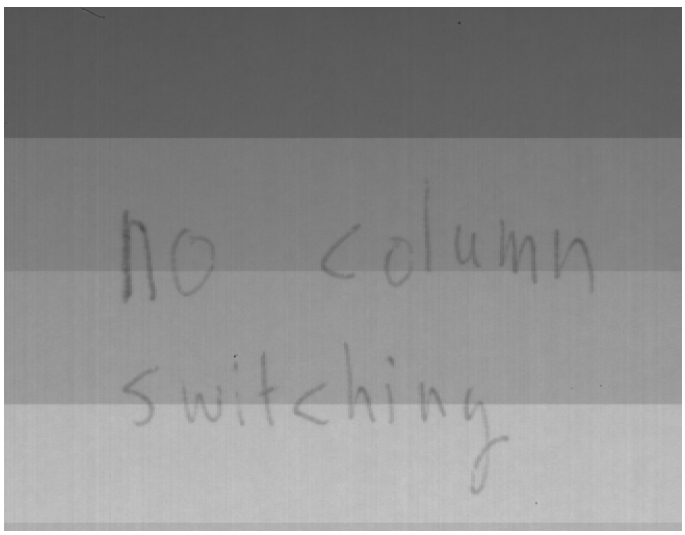

Figure 27.4.3: Raw image captured without using DCS.

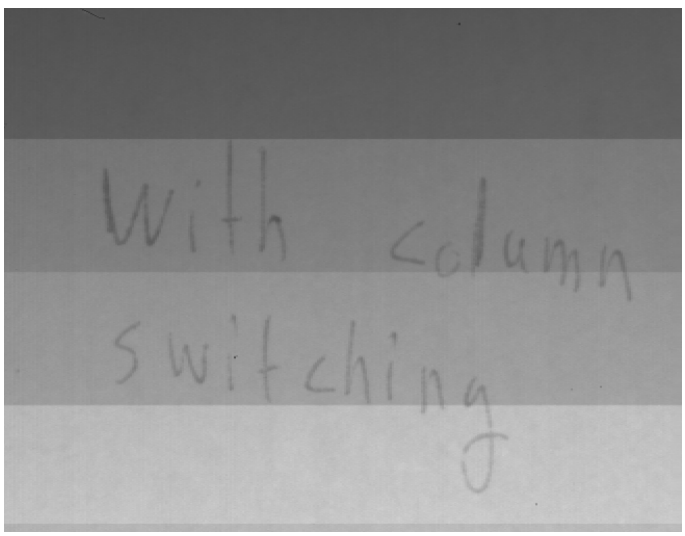

Figure 27.4.4: Raw image captured while using DCS.

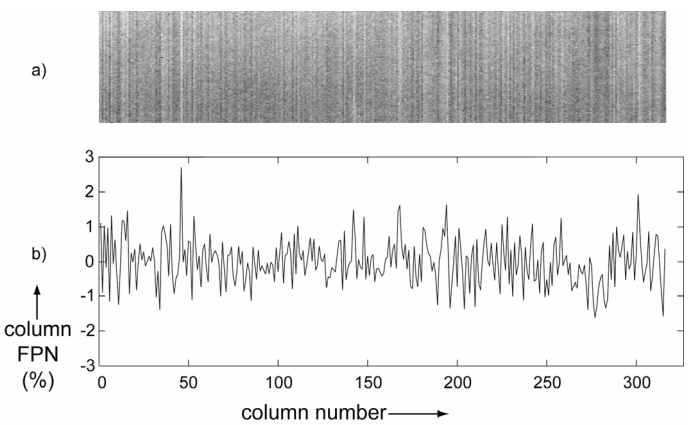

Figure 27.4.5: a) Contrast enhanced image region without DCS b) average column output,showing a column FPN of 0.67% (std. dev.).

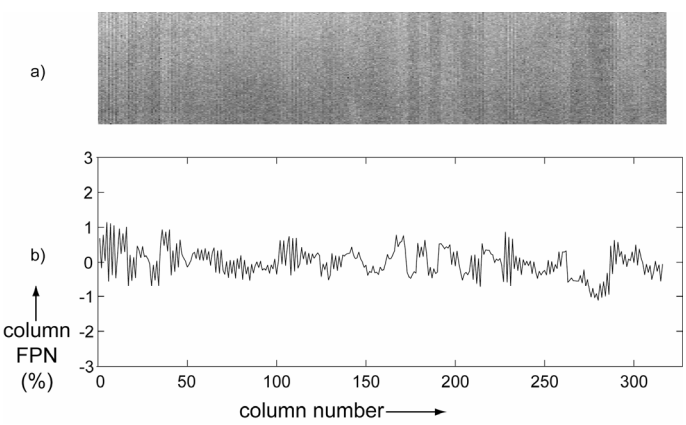

Figure 27.4.6: a) Contrast enhanced image region with DCS b) average column output, showing a column FPN of 0.41% (std. dev.).

Continued on Page 669

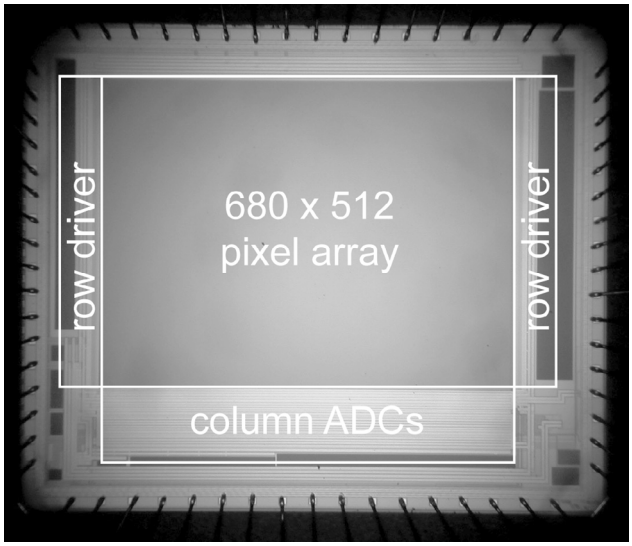

Figure 27.4.7: Chip micrograph of the prototype imager.

